A Unified Approach to the Design of Wide-Band Microwave Solid-State Oscillators

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Abstract—**Present design techniques for broad-band tunable MESFET and bipolar transistor oscillators are indirect and tedious. We present a new technique based on negative resistance concepts and a new theorem herein stated and proven. This technique is developed through two design examples: a 5.9–12.4-GHz MESFET oscillator and a 2–8.4-GHz bipolar transistor oscillator.**

I. Introduction

THE DESIGN of wide-band tunable microwave oscillators has long been an inexact science. The reasons are many. Microwave devices that exhibit appreciable gain in the 1- to 18-GHz frequency range are of relatively recent vintage. The gains of these devices typically drop rapidly with frequency. Also, most circuit elements in the microwave range act as distributed parameters. This has made both device characterization and accurate modeling difficult. Accurate characterization is possible only by the use of microwave network analyzers using s-parameter matrices. Unfortunately, the use of these matrices in oscillator design is not well developed. Oscillator design still tends to be cut-and-try: a topology is selected, and the existence and bandwidth of oscillations are verified empirically, either on the workbench or at the computer. Such design methods perforce preclude control over such parameters as power flatness, tuning linearity, harmonic distortion, and noise.

It is possible, however, to use the s matrices to advantage in the design of oscillators [1], [2]. To do this it is necessary to understand the relationship between the s matrix for a given topology, which includes an active device, and the oscillation conditions. Once these are understood, the design of oscillators becomes predictable and exact. Further, the tailoring of devices to obtain optimum performance becomes possible.

II. Negative Resistance

It is possible to develop negative resistance across two terminals in a variety of ways. Bulk effects, such as in transferred electron devices, and semiconductor junction effects, such as in tunnel or IMPATT diodes, can produce negative resistances of varying magnitude and frequency range. Certain combinations of three-terminal devices, feedback elements, and terminating elements can also produce negative resistance. We are motivated to use negative resistance analysis rather than closed form stability analysis by several considerations. Device gain and reverse isolation decrease rapidly with frequency. Circuit elements all have a distributed nature at microwave frequencies. Most importantly, the only accurate measurement technique available is network analysis which gives information in terms of forward and reflected waves which are one-port (two-terminal) parameters. Other motivations exist, as we will show now.

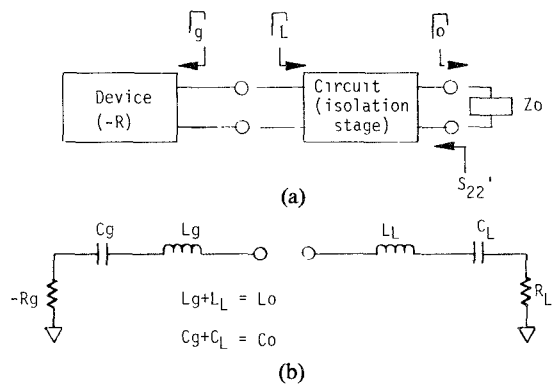

Fig. 1. Equivalent circuit for oscillation condition analysis.

To analyze a three-terminal device as a negative resistance, we choose a circuit topology which includes the device. We then inspect some port for the existence of negative resistance. Assume we have done this and that we can represent the equivalent circuit of the configuration around some frequency ω_0 by the series equivalent circuit shown in Fig. 1(b). With a load placed as shown, oscillation conditions are given by $j(X_L+X_g)=0$ and $R_L=-R_g$, or by $\Gamma_L\Gamma_g=1$, where Γ_L and Γ_g are the reflection coefficients produced by R_L+jX_L and R_g+jX_g. If $|R_L|<|-R_g|$, then the net resistance around the closed path is negative, and oscillations will start and build up until device nonlinearities and voltage and current limitations cause it to reach steady state. $-R_g$ can be accurately described by some nonlinear V–I relationship. We could represent it as a power series

$$V=(A_1)I+(A_2)I^2+(A_3)I^3+\cdots$$

so that $R_g=V/I=A_1+(A_2)I+(A_3)I^2\cdots$, with A_1 negative and $A_2, A_3,\cdots$ typically positive. Thus the magnitude of R_g decreases from its small signal value of A_1 to a value $-R_L$, at which point oscillations reach steady state. Note

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that, on a Smith chart representing the load plane, the region outside the A_1 resistance circle represents the oscillation region, and that inside is the stable region.

III. Induced Negative Resistance

For two-terminal (diode) negative resistance devices, the act of applying the proper dc bias is sufficient to generate negative resistance across the device terminals. In bipolar transistors and MESFET's, however, the negative resistance that leads to oscillations must be induced by the choice of proper feedback elements and terminating impedances. We illustrate this in the case of a MESFET by choosing as an example the common gate configuration that is very effective in YIG oscillator design.

Fig. 2 shows the oscillator configuration with the MESFET equivalent circuit incorporated. It can be shown that Z_{is}, the input impedance seen looking into the source with load Z_L, is given by

$$Z_{is} = R_s + Z_1$$

where

$$Y_1 = \frac{1}{Z_1} = \frac{1}{(Z_L + Z_d)} + \frac{1}{Z_g} + \frac{Z_d}{Z_L + Z_d} \cdot \frac{g_m}{Z_g \cdot j\omega C_g}. \quad (1)$$

Similarly, Z_{id}, the impedance looking into the drain with source load Z_s, is given by

$$Z_{id} = Z_d + Z_d \cdot (Y_g + Y_s)^{-1} \cdot \left(\frac{1}{Z_d} + \frac{g_m}{Z_g \cdot j\omega C_g} \right). \quad (2)$$

In both expressions, the negative resistance arises out of the fact that, for

$$\omega^2 L_g C_g > 1, \qquad \mathrm{Re}\left(\frac{g_m}{Z_g \cdot j\omega C_g} \right) < 0.$$

However, it is obvious that this is not sufficient to make Re $(Z_{is}) < 0$ or Re $(Z_{id}) < 0$. For this the negative impedance must be large enough to overcome terms containing Z_L and Z_s, respectively, in (1) and (2).

It can thus be seen that, at any given frequency, there exist values of Z_s (or Z_L) for which Z_{id} (or Z_{is}) have positive real values and others for which Z_{id} (or Z_{is}) have negative real values. Thus for given values of ω, L_g, C_g, Z_d, g_m, etc., trajectories of Z_L and Z_s can be drawn on the Smith chart that separate the regions that will and will not allow oscillations.

We can make a few other pertinent observations. So long as the equivalent circuit stays as simple as the above, we could even calculate the large signal values of the negative resistance as a function of signal level, if the variations of g_m, R_d, etc., with signal level are known or can be approximated. This would give us the coefficients A_i we needed in the previous section. A computer program would be the most convenient way to do this.

As the equivalent circuits get more complicated, however, the following more general method becomes necessary.

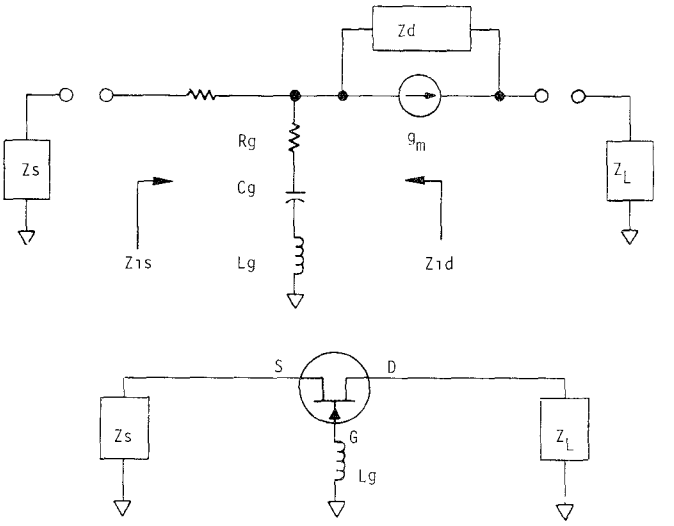

Fig. 2. Common gate oscillator configuration and equivalent circuit.

IV. Design Theory

Oscillator design is often done with devices whose equivalent circuits are not known but whose s parameters are measurable, or with multidevice structures that do not lend themselves to simple analysis. Also, in most cases, oscillator design proceeds one of two ways. In one, the tuning resonator is placed across one pair of terminals and the load across another. Alternately, the device can be imbedded in a circuit and only one pair of terminals brought out, in which case the load becomes a part of the frequency tuning circuit. In either case, some method to determine the circuit topology from the measured data is needed since closed form solutions are well nigh impossible.

To determine the oscillation conditions, it is useful to separate the load plane at both the input and output ports into regions that will exhibit negative resistance, and regions that will not. To do this we must somehow relate these regions to the s matrix of the two-port. This we do by means of the following theorem.

Theorem

Consider the two-port in Fig. 3 represented by an s matrix whose elements are S_{11}, S_{12}, S_{21}, and S_{22}. Let a reflection coefficient Γ_1 placed at port 1 result in a port 2 input reflection coefficient of S'_{22}, and a reflection coefficient Γ_2 placed at port 2 result in a port 1 input reflection coefficient of S'_{11}. Then the oscillation conditions $S'_{11}\Gamma_1 = 1$ and $S'_{22}\Gamma_2 = 1$ simultaneously represent boundary conditions for the two-port to generate oscillations, i.e., $S'_{11}\Gamma_1 = 1$ if and only if $S'_{22}\Gamma_2 = 1$.

Proof: From

$$S'_{22} = S_{22} + \frac{S_{12}S_{21}\Gamma_1}{1 - S_{11}\Gamma_1}$$

we can show that

$$\frac{1}{S'_{22}} = \frac{1 - S_{11}\Gamma_1}{S_{22} - |s|\Gamma_1}$$

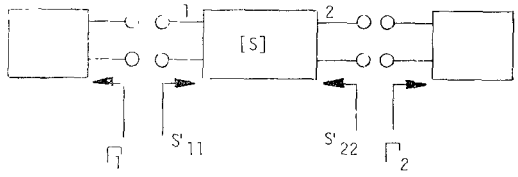

Fig. 3. Theorem block diagram.

where $|s|$ is the determinant of the s matrix. Substituting for S_{11} from

$$S_{11} = S'_{11} - \frac{S_{12}S_{21}\Gamma_2}{1 - S_{22}\Gamma_2}$$

we get

$$\frac{1}{S'_{22}} = \frac{(1 - S'_{11}\Gamma_1) + \dfrac{S_{12}S_{21}\Gamma_1\Gamma_2}{1 - S_{22}\Gamma_2}}{S_{22}(1 - S'_{11}\Gamma_1) + \dfrac{S_{12}S_{21}\Gamma_1}{1 - S_{22}\Gamma_2}}.$$

Set $S'_{11}\Gamma_1 = 1$ (threshold of oscillations); then

$$\frac{1}{S'_{22}} = \frac{S_{12}S_{21}\Gamma_1\Gamma_2}{S_{12}S_{21}\Gamma_1} = \Gamma_2$$

i.e.,

$$S'_{22}\Gamma_2 = 1.$$

Similarly, we can show that if $S'_{22}\Gamma_2 = 1$, then $S'_{11}\Gamma_1 = 1$.

Let us consider the implications of the theorem. For every Γ_2 there corresponds some S'_{11} and, for the case where the Γ_2 chosen results in oscillations, there exists some value of Γ_1 such that $\Gamma_1 S'_{11} = 1$. Moreover, this value of Γ_1 corresponds to a value of S'_{22} such that $\Gamma_2 S'_{22} = 1$.

In the design of oscillators, we ask ourselves the following questions. 1) Is there a set of loads that can be placed at port 1 that will have the effect of causing oscillations? 2) If so, are there loads that can be placed at port 2 that will enhance or can inhibit such oscillations? 3) What, in fact, would be the loads at ports 1 and 2 that give the desired performance?

One way of proceeding to obtain answers would be as follows. We assume that we can synthesize any passive load we wish at port 2; i.e., we can generate any load such that $|\Gamma_2| \leqslant 1$. ($|\Gamma_2| = 1$ represents a boundary circle for the load at port 2.) Since the s matrix is a bilinear transformation, $|\Gamma_2| = 1$ maps into a circle in the S'_{11} plane. The condition $\Gamma_1 S'_{11} = 1$ represents a further bilinear transformation that maps the circle in the S'_{11} plane into a circle in the Γ_1 plane defined by $\Gamma_1 = 1/S'_{11}$. Thus $|\Gamma_2| \leqslant 1$ and the condition $\Gamma_1 S'_{11} = 1$ combine to generate a circle in the Γ_1 plane, which represents the boundary conditions for oscillations, for oscillations are possible either within this circle or without, but not in both places. Let this circle be represented by the equation $|\Gamma_1 - \boldsymbol{a}| = b$ where b is the radius of the mapped circle and $\boldsymbol{a}$ its vector offset from the origin. Consider first the case where the area defined by $|\Gamma_2| \leqslant 1$ maps within this circle. Then for any point $X \in |\Gamma_2| < 1$, there exists a point $Y \in |\Gamma_1 - \boldsymbol{a}| < b$, such that $\Gamma_1 S'_{11} = 1$.

To answer question 1, then, we have only to investigate whether $|\Gamma_1 - \boldsymbol{a}| = b$ intersects, contains, falls within or outside of $|\Gamma_1| \leqslant 1$. If it intersects or falls within, a passive $|\Gamma_1| < 1$ exists such that $\Gamma_1 S'_{11} = 1$, so a load Z_1 can be synthesized that will cause oscillations at ω_0. The area within the intersection of the two circles in fact denotes the impedances Z_1 that make oscillations at port 1 possible. If $|\Gamma_1 - \boldsymbol{a}| = b$ falls outside of $|\Gamma_1| \leqslant 1$, however, it would require a negative resistance load of sufficient magnitude and phase to create oscillations at port 1.

Now consider the case where $|\Gamma_2| \leqslant 1$ maps outside the circle $|\Gamma_1 - \boldsymbol{a}| \leqslant b$; then any Γ_1 outside the circle $|\Gamma_1 - \boldsymbol{a}| \leqslant b$ will cause oscillations at port 1. For there to exist passive loads such that oscillations are possible, it is only necessary that $|\Gamma_1 - \boldsymbol{a}| \leqslant b$ not enclose the area $|\Gamma_1| \leqslant 1$.

Now that we have answered question 1, we can proceed to the second question. To do this we determine the map of the $|\Gamma_1| \leqslant 1$ into the Γ_2 plane, given by, say, $|\Gamma_2 - \boldsymbol{c}| \leqslant d$. As in the previous case, the relation between this circle and $|\Gamma_2| \leqslant 1$ determines the oscillation conditions at port 2. The third question is answered by the use of the actual Γ_1 chosen at port 1, for example, and by designing the proper match at port 2 for desired performance.

A question that arises is what happens when there is considerable isolation between the oscillator stage and the output port. Since all the stages could be lumped into an s matrix, the $\Gamma_i S'_{ii} = 1$ conditions still determine the boundary of oscillations.

Let the region inside the circle $|\Gamma_1 - \boldsymbol{a}| = b$ represent oscillation conditions. Also, let this intersect the $|\Gamma_1| = 1$ circle. With sufficient isolation the region outside $|\Gamma_2 - \boldsymbol{c}| = d$ would represent oscillation conditions, for port 2 with $|\Gamma_2 - \boldsymbol{c}| = d$ falling outside the $|\Gamma_2| = 1$ circle. To stop oscillations at port 2, we would need to produce a Γ_2 that falls within $|\Gamma_2 - \boldsymbol{c}| = d$. Stated otherwise, it would need reflection coefficient $\Gamma_2 \epsilon (|\Gamma_2 - \boldsymbol{c}| \leqslant d)$ at the output port (i.e., some massive negative resistance load) to reflect a S'_{11} at port 1 such that $\Gamma_1 S'_{11} = 1$ is not possible for any $|\Gamma_1| \leqslant 1$.

An important consequence of the theorem is that a step-by-step oscillator design procedure gets automatically defined. The procedure is stated as follows.

1) Place the resonator to be used, including losses, at, say, port 1 and plot S'_{22} through the resonance. Do this at many different frequencies in the desired band.

2) Plot $1/S'_{22}$ through the resonance at all the frequencies. This will separate the Smith chart at each frequency into two regions—one in which oscillations will not occur and the other in which oscillations will. Which is which can be determined by a single point check on the computer.

3) Determine an acceptable load contour. Here, physical realizability, producibility, oscillation margin, power output, linearity, etc., will become considerations.

4) Verify $\Gamma_1 S'_{11} > 1$ for the load selected. This is conveniently done by plotting the resonator circle and verify-

ing that $(1/S'_{11})^*$ falls within the circle for each frequency.

The next two sections give examples of two such designs, and how the various design tradeoffs are analyzed and utilized.

V. Design Example: MESFET Oscillator

This section presents the application of the preceding theorem and techniques to the design of a 5.9–12.4-GHz YIG-tuned MESFET oscillator. The first consideration in three-terminal-device oscillators is the choice of negative-resistance-generating topology. We need a very broadband negative resistance which meets the reactance constraints of the resonator. For a YIG, which is inductively coupled, we must avoid capacitive reactance, for this could lead to a fixed frequency resonance which would inhibit tuning range. The topology which best meets these constraints is the common gate (or in the bipolar case, common base) topology shown in Fig. 4. Once this choice is made, the design proceeds as follows:

1) characterize the resonator and derive an equivalent circuit;
2) characterize the FET and derive an s matrix or an equivalent circuit;
3) connect these as shown in Fig. 4(a) and analyze the output impedance versus frequency around the resonator's resonance;
4) plot $1/S'_{22}$ versus frequency for all the frequencies of interest.

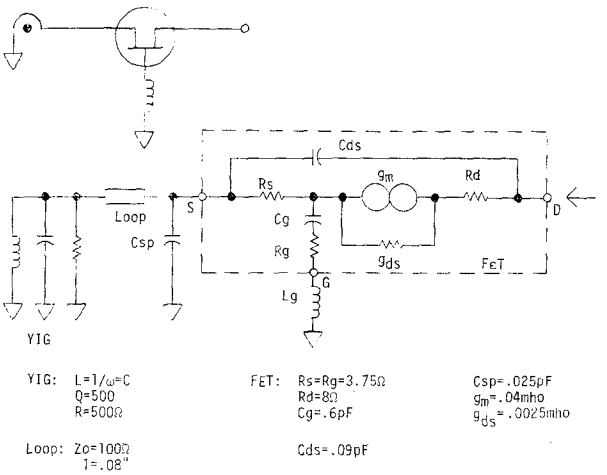

Fig. 4. MESFET oscillator configuration and circuit model.

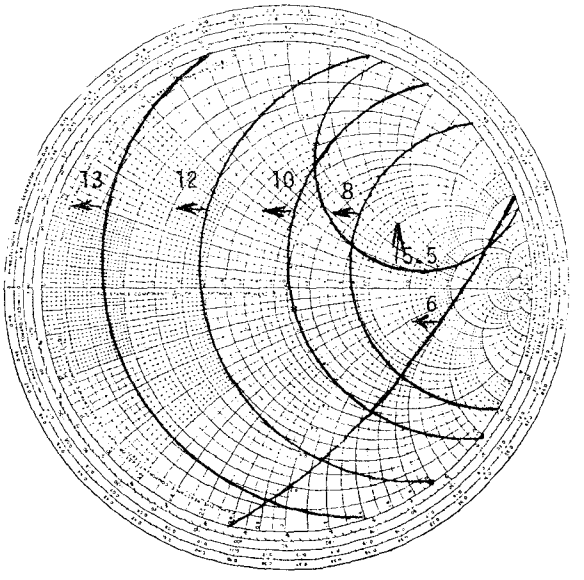

Fig. 5. Oscillation conditions for circuit in Fig. 4. Contours of Γ_2 defined by $S'_{22}\Gamma_2 = 1$. The frequencies are in gigahertz.

The pertinent equivalent circuit is shown in Fig. 4(b), and the resulting contours are shown in Fig. 5. The regions shown by arrows are the load impedances which will enable this circuit to oscillate at the given frequency.

Experimental confirmation of these contours was accomplished using the load-pull setup in Fig. 6. This system [4] allows simultaneous monitoring of the impedance the device sees and power, frequency, noise, or any other parameter of interest. The experimental procedure for generating contours of constant power is to present a variety of loads to the oscillator and note the power at that load on a Smith chart. Common points can be connected into contours.

The results of this procedure for this example are shown in Fig. 7. An interesting observation is that the optimum power match point is identical to that of an amplifier, provided the oscillation condition is met at that load (i.e., 8 and 10 GHz). If the oscillation condition is not met, the optimum power occurs at a load as close to Z opt as possible, with power derated by the mismatch from Z opt. Another observation is that as the power output decreases from maximum, the corresponding contour presents a closer and closer approximation to the contour that defines the oscillation condition limit for that frequency. This can be verified by comparing Fig. 7 to Fig. 5. The differences are ascribable to parasitics not accounted for in the model.

From these contours a design procedure for power and bandwidth is immediately apparent: a load trajectory which intersects the contour centers versus frequency is required. Note that this case requires an anti-Foster trajectory which one can only approximate. Since no analytic design technique exists for this problem, some other approach must be derived. Consider the basic circuit topology shown in Fig. 8. All of the circuit elements are required to bias the devices, separate them physically for assembly and thermal reasons, and provide stability for the amplifying device. This topology also has features which have potential for achieving the desired impedance function; the "separation" and "*Vds*" lines form an inductive transformer, and the blocking capacitor helps to absorb the input capacitance of the second FET. From this point, the design proceeds to the computer in one of two ways: first, using a match optimization program, it is possible to arrive at a particular impedance trajectory by using the optimizer's cost function to shift the matching goals as a function of frequency. Alternately, an interactive program could be used wherein the designer would

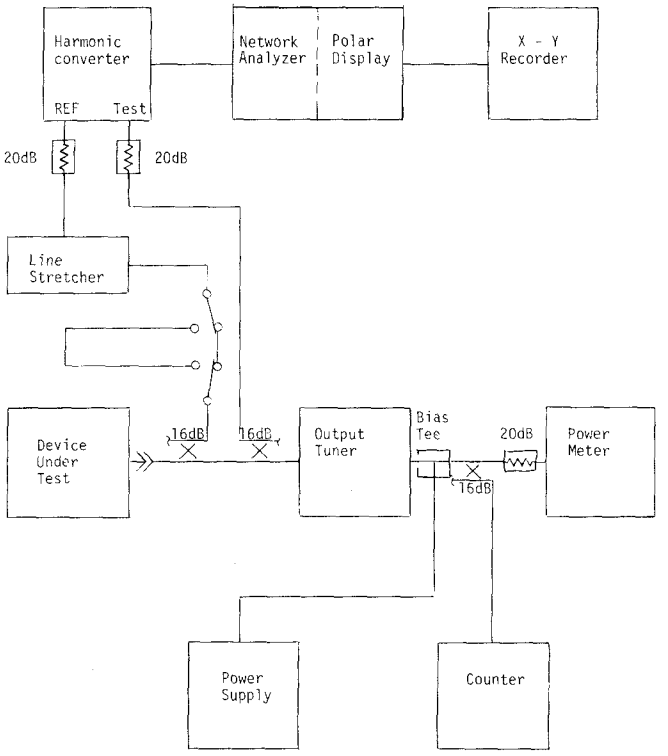

Fig. 6. Load-pull setup.

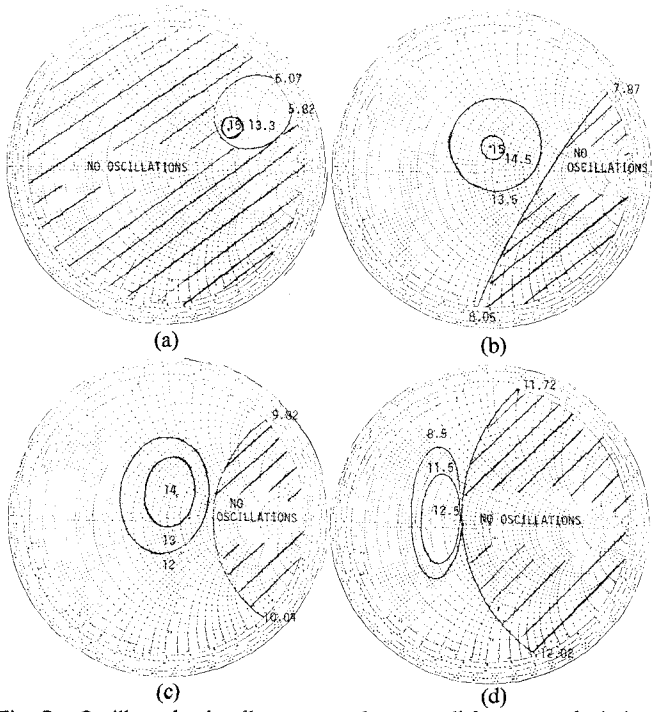

Fig. 7. Oscillator load-pull power results at small frequency deviations centered around (a) 6 GHz, (b) 8 GHz, (c) 10 GHz, (d) 12 GHz. Power results are in dBm.

"tweak in" the element values to achieve the desired trajectory.

Finally, device parameter fluctuations which affect the oscillation conditions and the match must be considered. The two tuning lines shown in Fig. 8 achieve this. The "low end tuning" compensates for oscillator device capacitance to achieve negative resistance over the proper band, and the "high end tuning" compensates for both the oscillator device and the input impedance of the amplifier device to achieve the negative resistance to the desired upper band edge.

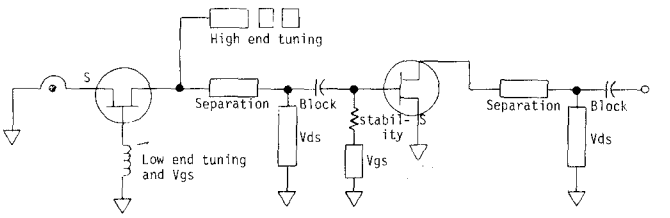

Fig. 8. MESFET oscillator minimal topology.

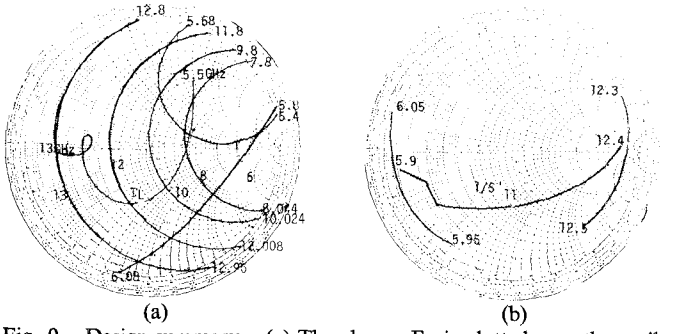

Fig. 9. Design summary. (a) The chosen Γ_L is plotted over the oscillation condition contours. (b) $1/S_{11_s}$ is plotted with portions of Γ_{YIG} at the band edges. All frequencies are in gigahertz.

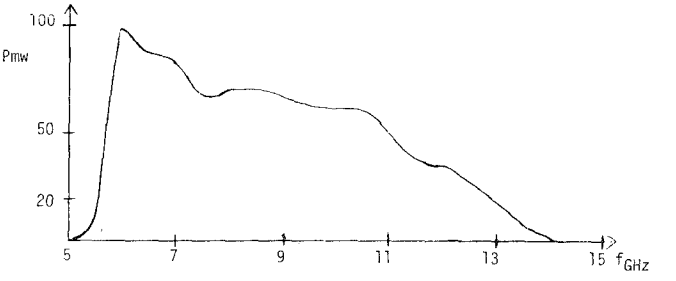

Fig. 10. MESFET oscillator power versus frequency.

The amplifier stage is used to compensate for oscillator power rolloff and to buffer the oscillator device from the load. Note that synthesis techniques fail us in the amplifier stage design because reflective or absorptive gain compensation results in nonoptimum terminations for maximum power transfer out of this device. We must design an impedance trajectory which yields the exact gain/power tradeoff needed by the systems application.

A summary of the design results is shown in Fig. 9. In Fig. 9(a), the theoretical oscillation condition contours are reproduced along with the match presented to the oscillator device to meet these oscillation conditions. In Fig. 9(b), the inverse of the input impedance of the oscillator device is plotted. Also plotted are the impedance contours of the resonator including losses at the band extremes. It can be seen that there is sufficient negative resistance to overcome resonator losses everywhere in band [5].

Fig. 10 shows the typical swept performance of this oscillator. It covers 5.5–14.1 GHz with 15-dBm minimum power from 5.9–12.4 GHz. Harmonics are better than −20 dBc.

VI. Design Example II—Bipolar Oscillator

These identical techniques can be applied to the design of a 2–8.4-GHz YIG-tuned bipolar oscillator. Fig. 12(a) shows the oscillation load plane contours for an in-house 1-μm emitter finger bipolar device with 0.8 nH of base inductance. These were generated using the resonator model and measured s parameters of the transistor. Superimposed on the load plane is the impedance trajectory arrived at using the topology of Fig. 11 to achieve oscillations over the full band. Fig. 12(b) shows $1/S'_{11}$ to demonstrate that the resonator losses are swamped out by the oscillator negative resistance. The amplifier considerations are the same as the previous design example, hence, the similarity of topologies.

An interesting technique can be used to generate flat output power. If S_{21} is analyzed from the emitter of the bipolar device through the FET to the output, this closely approximates the amplitude shape of the final unit. Some flexibility exists in achieving impedance trajectories at the collector for oscillators so this can be tailored for flat S_{21}. The same technique can be applied to the previous design example, but it is less successful in predicting amplitude shape than in the bipolar case.

Fig. 13 depicts the performance of this oscillator; typically, it sweeps from 1.8–9.3 GHz with 12-dBm minimum power from 2–8.4 GHz and harmonics better than −20 dBc.

VII. Device–Circuit Interface—Specifying the Oscillator Device

In a production environment, it is essential that an oscillator design accomodate a wide range of devices, and that the relationship between device parameter fluctuations and circuit performance fluctuations be well defined. To this end, we will present a technique for defining this interface which is also useful for extrapolating device requirements for future designs.

Recalling the FET model of Fig. 4, consider g_m, C_g, R_d, and the total input resistance which we shall call R_{gs} to be parameters which characterize a given FET; all other elements of the device model are considered invariant from one device to another. To determine the effect of parameter shifts, we need a figure of merit to quantize these shifts. In an amplifier, this might be minimum gain or maximum noise figure across a band; in an oscillator, it would be the negative resistance bandwidth. Now we want to develop a table of FET's with different parameters but a constant figure of merit. To do this, we use a computer model of the oscillator and cycle devices through it, varying their parameters and observing the resultant negative resistance bandwidth. Table I shows the results of this study on the aforementioned MESFET oscillator.

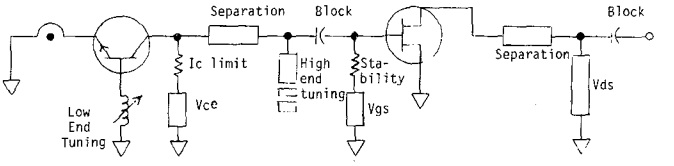

Fig. 11. Bipolar oscillator minimal topology.

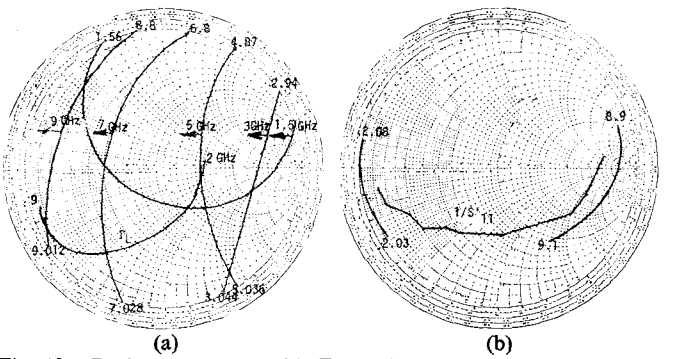

Fig. 12. Design summary. (a) Γ_L and oscillation conditions. (b) $1/s'_{11}$ and Γ_{YIG}. All frequencies are in gigahertz.

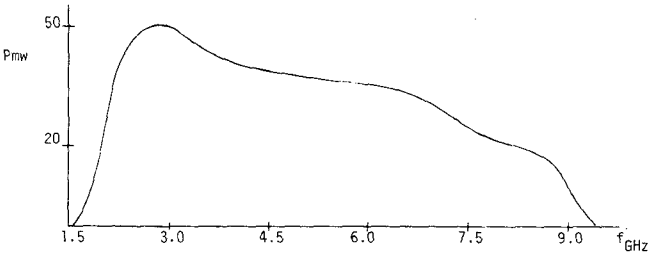

Fig. 13. Bipolar power versus frequency.

TABLE I

gm	Cg	Rgs	1/gds	Figure of Merit
.040	.4	10	240	Constant
.040	.5	10	260	"
.040	.6	10	300	"
.040	.7	10	400	"
.040	.8	10	500	"
.0325	.4	10	300	"
.036	.5	10	300	"
.0425	.7	10	300	"
.047	.8	10	300	"
.040	.4	20	300	"
.040	.5	13.5	300	"
.040	.7	7.5	300	"
.040	.8	5	300	"
.040	.6	5	225	"
.040	.6	16	400	"
.040	.6	24	600	"
.048	.6	10	200	"
.035	.6	10	400	"
.030	.6	10	600	"
.034	.6	5	300	"
.044	.6	16	300	"
.052	.6	24	300	"

Given a set of different FET's with like figures of merit, a formulation can be derived which will predict whether other devices will be adequate for the application in question. One such formulation is a modified[1] f_{max} form:

[1] f_{max} results if $A=1$ and $B=C=0.5$.

$$\frac{g_m^A R_d^B}{C_g R_{gs}^C} \geqslant K.$$

A computer program was written to take the table of FET's and curve fit them to this form by varying A, B, C, and K until $\Sigma \Delta K / \bar{K}$ is a minimum.

Some results of equations which result from this analysis follow.

1) 5.9–12.4-GHz oscillator:

$$\frac{g_m^{1.6} R_d^{0.6}}{C_g R_{gs}^{0.3}} \geqslant 0.3.$$

2) 5.9–12.4-GHz amplifier:

$$\frac{g_m^{1.2} R_d^{0.125}}{C_g R_{gs}^{0.25}} \geqslant 0.037.$$

If the value of the oscillator expression is greater than 0.3, that implies a stronger oscillator with excess bandwidth. If the amplifier expression is greater than 0.037, that implies greater gain. In fact, these expressions can be used to predict accurately the bandwidth and gain, respectively, of the two circuits given the FET parameters.

An interesting sidelight for FET oscillators emerged upon examination of the device requirements for three different oscillators; if we force the expression into the $f_{\max}$ form, the following relationship ensues:

$$fh^2/fl = f_{\max}$$

where fl is the lower oscillation band edge and fh is the upper oscillation band edge. We can use this expression to extrapolate oscillators and pick FET's to start designs.

A strength of this technique with FET's is the ability to use it as a guide in tailoring devices to a given application. For example, it might be feasible to screen to a higher value of g_m if wider bandwidth is desired. The model parameters in an FET relate closely to process parameters. In bipolar transistors, however, no such simple model exists. The technique can still be used in an s-parameter form to generate a device screening equation, but the coupling between device process parameters and s parameters is very light.

VIII. Conclusion

We have demonstrated the utility and advantages of a negative resistance approach to the design of three-terminal device broad-band tunable oscillators at microwave frequencies. The theorem we presented and its consequences lead to a well-defined design procedure. The theorem has been verified by mathematical proof, empirical (load-pull) data, and two actual oscillator designs. Finally, we have presented a technique for specifying and optimizing devices for oscillator applications.

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